BIT PROCESSING METHOD FOR ADAPTIVE MULTIRATE MODULATION

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CROSS REFERENCE TO RELATED APPLICATION

[0001] Pursuant to 35 U.S.C. § 119(a), this application claims the benefit of earlier filing date and right of priority to Korean Patent Application No. 2002-67239, filed on October 31, 2002, the content of which is hereby incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates a radio communication system and, more particularly, to a discontinuous transmission (DTX) bit processing method for an adaptive multirate modulation.

Description of the Related Art

[0003] With the emergence of the information society, the center of services of telecommunication field is shifted from the low speed voice communication service to a multimedia service providing audio, video as well as voice communication. In order to support multimedia services that require high speed data transmission, it is critical to maximize the channel capacity by effectively utilizing the limited resources such as power and frequency band.

[0004] For effective utilization of the limited resources, various modulation techniques have been developed. In case of a wired network, channel characteristics are stable so that high efficiency QAM modulation/demodulation

techniques are widely used. A radio network, generally, is not stable compared to the wired network, due to multipath transmission and fading according to a Doppler effect. A frequency shift keying (FSK) or a phase shift keying (PSK) modulation in which 1~2 bits are transferred per 1 Hz. However, recently, with the development of the modulation technique, a multirate modulation scheme such as 16-QAM, 64-QAM, or the like is adopted even in the radio network.

[0005] The current and undergoing radio communication systems in the domestic and foreign countries are likely to adopt a fixed modulation scheme regardless of a channel state between the base station and the subscriber. Such a system has a problem in that that a low rate modulation scheme is used, even when a high rate modulation can be used in a good channel state, resulting in failure of maximization of the system capacity.

[0006] Also, the system adopting the fixed modulation scheme can not change the modulation rate such that the same low rate modulation is used even when the channel state is bad. Accordingly, the transmission quality is further degraded, and causes the communication channel to break.

[0007] In order to solve the above problems, the 3rd Generation Partnership Project (3GPP) standard conference has discussed a High speed Downlink Packet Access (HSDPA) on the basis of an adaptive modulation.

[0008] In the quadrature phase shift keying (QPSK) modulation, the DTX bit can be allocated to one of In-Phase (I) and quadrature (Q) axes in the IQ plane so that the transmission rate can be decreased by turning off the transmission power to the axis to which the DTX bit is allocated.

[0009] Since the discussion on the HSDPA proceeded, the multirate modulation scheme such as the QAM (Quadrature Amplitude Modulation) that generates four bits out of one baud has been adopted for flexible modulation, in

which the DTX bit allocation as in the QPSK is not adopted. In the HSDPA of the 3GPP standard, a multirate modulation such as 16-QAM or 64-QAM as well as the QPSK, is used. In the case of the multirate modulation, a problem is how to process the DTX bits. In this regard, Mitsubishi has proposed a DTX bit processing method in which DTX bits are bound into one symbol and then mapped into the origin of an IQ plane.

[0010] FIG. 1A, FIG. 1B, FIG. 2A, and FIG. 2B illustrate the DTX bit processing method proposed by the Mitsubishi. As shown in FIG. 1A, the empty region of a frame is bound into a 4 bit DTX symbol and then the DTX symbol is mapped to the origin of the IQ plane (see FIG. 1B). In FIG. 2A and FIG. 2B, the empty region of a frame is allocated into each 4 bit symbol to be transmitted by 2 bits such that only 4 symbol points of the IQ plane are used for transmit.

[0011] The above DTX bit processing method has a drawback in that this method may not be compatible with the currently developing system since this method requires modification of the current multiplexing scheme. Also, it is very complicated to implement the algorithm in which DTX bits are grouped in one symbol so as to be mapped to the origin or 2 bits are inserted into each data symbol so as to be transmitted using only four symbol points on the IQ plane.

SUMMARY OF THE INVENTION

[0012] A bit processing method for a multirate modulation scheme is provided. The method comprises receiving a symbol; determining whether the symbol comprises at least one DTX bit; mapping the symbol to a predetermined mapping point (S) on an IQ plane; minimizing a transmission power level if the symbol has at least one DTX bit; and transmitting the symbol in the transmission power level of the mapping point.

[0013] The mapping point is calculated by averaging signal points in which bits corresponding to non-DTX bits of the symbol are identical with each other on the IQ plane. The mapping point is set in consideration of at least one of a number of the non-DTX bits, a number of the selected signal points, and locations of the selected signal points on the IQ plane. The symbol is mapped to an origin of the IQ plane, when all bits of the symbol are DTX bits.

[0014] The symbol is mapped to a signal point in which bits are identical with the bits consisting of the symbol on the IQ plane when the symbol has no DTX bit. The mapping point is set in consideration of plus and minus symbols of the signal points on the IQ plane. In some embodiments, the mapping point is set in consideration of at least one of number of the non-DTX bits, number of the selected signal points, and locations of the selected signal points on the IQ plane.

[0015] In certain embodiments, the symbol is mapped to an origin of the IQ Plane, when all bits of the symbol are DTX bits. The symbol is mapped to a signal point of which bits are identical with the bits comprising the symbol on the IQ plane, when the symbol has no DTX bit. In one embodiment of the present invention, a DTX bit processing method reduces the transmission power consumption by mapping a symbol having DTX bits to a predetermined signal point, on an IQ plane.

[0016] These and other embodiments of the present invention will also become readily apparent to those skilled in the art from the following detailed description of the embodiments having reference to the attached figures, the invention not being limited to any particular embodiments disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The accompanying drawings, which are included to provide a

further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0018] FIG. 1A illustrates a conventional method for allocating DTX bits into symbols in accordance with one or more embodiments;

[0019] FIG. 1B illustrates how a symbol having DTX bits of FIG. 1A is mapped on an IQ plane in accordance with one or more embodiments;

[0020] FIG. 2A illustrates a conventional method for allocating DTX bits into symbols in accordance with one or more embodiments;

[0021] FIG. 2B illustrates how a symbol having DTX bits of FIG. 2A is mapped on an IQ plane in accordance with one or more embodiments;

[0022] FIG. 3 is a schematic view illustrating a transmitter of a base station modem adopting a DTX bit processing method in accordance with one embodiment of the present invention;

[0023] FIG. 4A is an exemplary constellation diagram of a 16-QAM in accordance with one embodiment;

[0024] FIG. 4B illustrates how a symbol having DTX bits is mapped on an IQ plane in accordance with one embodiment of the present invention; and

[0025] FIG. 5 is a flowchart illustrating a DTX bit processing method in accordance with one embodiment of the invention.

[0026] Features, elements, and aspects of the invention that are referenced by the same numerals in different figures represent the same, equivalent, or similar features, elements, or aspects in accordance with one or more embodiments of the system.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] Referring to FIG. 3, a transmitter of a base station modem

comprises a transport channel (TrCH) multiplexer 10 for multiplexing radio frames from each TrCHs into a composite transport channel (CCTrCH); a DTX insertion module 20 for inserting DTX bits into the radio frames of the CCTrCH; a physical channel segmentation module 30 for segmenting the CCTrCH for different physical channels (PhCHs); an interleaver 40 for interleaving the segments; and a PhCH mapping module 50 for mapping the segments to the corresponding PhCHs.

[0028] FIG. 4A is a typical constellation diagram of a 16-QAM and FIG. 4B is a constellation diagram for illustrating how a symbol having DTX bits is mapped on an IQ plane in accordance with the present invention. As shown in FIG. 4A, 4 bits are allocated to determine a symbol in the 16-QAM (as a matter of course, 6 bits are to be allocated in the 64-QAM), for example. Accordingly, one to four DTX bits can be allocated to the symbol.

[0029] In the multirate modulation of MQAM, 'M' is the exponentiation value of 2. Accordingly, 1 to m DTX bits can be inserted into one symbol. DTX bits can be positioned in the symbol modulated by MQAM according to the number of DTX bits. In some embodiments, the symbol in which M bits are DTX bits is mapped to the origin of the IQ plane and the symbol including DTX bit(s) less than M are mapped to a predetermined signal point, on an IQ plane. The IQ plane is defined by averaging vectors of the signal points. The bits corresponding to the non-DTX bits of the symbol are identical with each other, in consideration of the quadrants to which the signal points are located, for example.

[0030] Referring to FIG. 4B, when a symbol having, for example, a bit order of 1XX0 (X is DTX bit) is inputted, 4 signal points (e.g., 1000, 1010, 1100, and 1110) are selected on the IQ plane. The left most bit and the right most bit can be identical with each other. The vector values of the 4 signal points are averaged so as to obtain a mapping point (S). Accordingly, the symbol of 1xx0 is mapped to the

mapping point (S).

[0031] In the same manner, when, for example, a symbol of 1XXX is inputted, eight signal points (i.e., 1011, 1001, 1010, 1000, 1110, 1100, 1111, and 1101) of which the left-most bit is one, and others are DTX bits are selected and averaged for calculating the mapping point (S). The mapping point (S) for the symbol of 1xxx is defined in consideration of the number of the non-DTX bit, the number of the selected signal points, and the locations of the selected signal points on the IQ plane so as to distinguish from the mapping point for the symbol of 1xx0. In certain embodiments, the symbol in which all the bits are DTX bits is mapped to the origin of the IQ plane. For example, 16QAM is adopted in one embodiment.

[0032] FIG. 5 is a flowchart illustrating the DTX bit processing method in accordance with one embodiment of the present invention. In FIG. 5, when 2^M bit QAM modulated signal is inputted to the DTX insertion module 20 from the TrCH multiplexer 10, the DTX insertion module 20 inserts DTX bits into the signal to be transmitted, if required. After passing through the DTX insertion module 20, the signal is segmented by the physical channel segmentation module 30, interleaved by the interleaver 40 and then transmitted to the physical channel mapping module 50 (at step S101), for example.

[0033] The physical channel mapping module 50 determines whether or not there exists DTX bit(s) in the input signal (step S102). In some embodiments, if there is a DTX bit in the symbol, the physical channel mapping module 50 selects the signal points in which the bit(s) corresponding to the non-DTX bit(s) of the symbol is/are, for example, identical with each other on the IQ plane (step S103) and averages the vectors of the signal points on the basis of the I and Q axes of the IQ plane so as to define a mapping point (S) (step S104). In this case the mapping point (S) is defined in consideration of the number of the non-DTX bit, the number of

the selected signal points, and the locations of the selected signal points on the IQ plane.

[0034] Subsequently, the physical channel mapping module 50 maps the symbol to the mapping point (S) (step S105) and transmits the symbol in the power level associated to the mapping point (S) (step S106). The symbol in which all the bits are DTX bits is mapped to the origin of the IQ plane.

[0035] In certain embodiments, in the DTX bit processing method, the symbol having the DTX bit(s) is mapped into a mapping point which requires a low transmission power level such that it is possible to minimize the transmission power consumption without modifying the typical modulation scheme for the HSDPA system.

[0036] Also, the DTX bit processing method of the present invention has an advantage in that the DTX bit processing algorithm can be simply implemented and easily applied to the actual communication system since that does not require any modification in the conventional modulation algorithm.

[0037] The embodiments described above are to be considered in all aspects as illustrative only and not restrictive in any manner. Thus, other exemplary embodiments, system architectures, platforms, and implementations that can support various aspects of the invention may be utilized without departing from the essential characteristics described herein. These and various other adaptations and combinations of features of the embodiments disclosed are within the scope of the invention. The invention is defined by the claims and their full scope of equivalents.